

RG85539C
SmartMedia Controller
Specifications

Rev. 2.0

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RATOC Systems, Inc.

Notice : Information in this document is subject to change without notice



1. Introduction

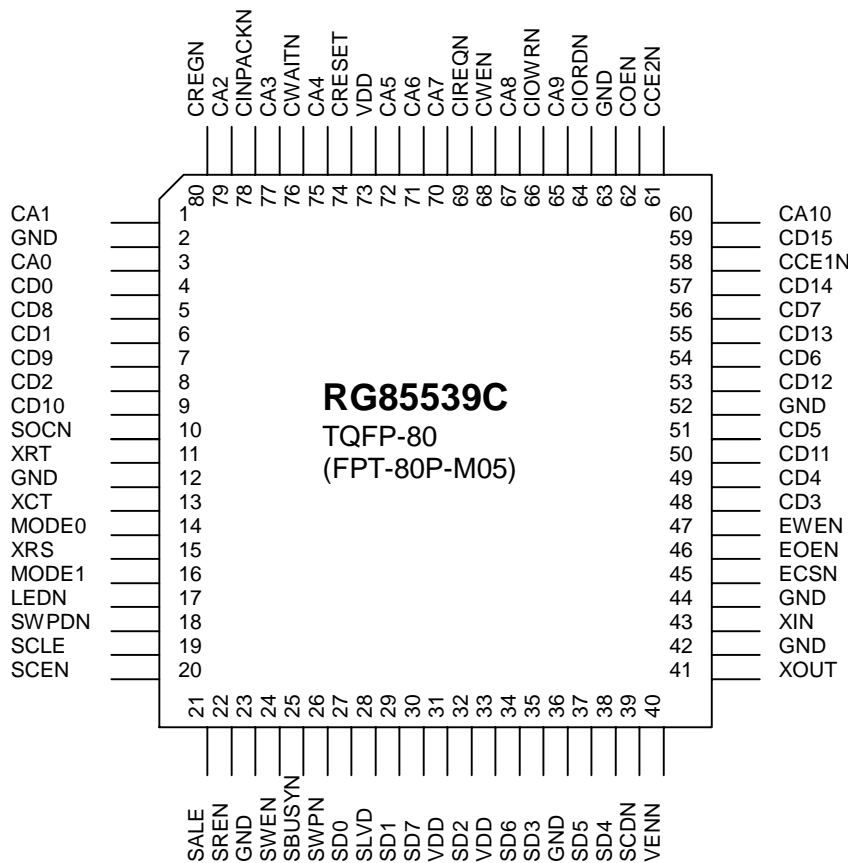
This is the controller which interfaces a SmartMedia SSFDC(Solid State Floppy Disk Card) and any kinds of buses.

2. Features

- Supports PC Card interface bus, Parallel interface bus (PRINTER-PORT), MPU bus.
- Supports both 3.3V and 5V SmartMedia cards.
- Detects and controls Vcc of SmartMedia.
- Supports Hot-Swapping.
- Access LED control circuit.
- Package TQFP80(FPT-80P-M05)
- Power supply of 5V (from -5 to +5%)

3. Pin assignment

1. Top view



2. Pin names

| Pin | Pin Name | | | Pin | Pin Name | | |
|-----|----------------|----------|---------|-----|---------------------|----------|---------|
| | PC Card | Parallel | MPU bus | | PC Card | Parallel | MPU bus |
| 1 | CA1 | N.C | MA1 | 41 | XOUT | | |
| 2 | GND | | | 42 | GND | | |
| 3 | CA0 | N.C | MA0 | 43 | XIN | | |
| 4 | CD0 | PD0 | MD0 | 44 | GND | | |
| 5 | CD8 | N.C | MD8 | 45 | ECSN/ESCS /EMODE | PSLCT | N.C |
| 6 | CD1 | PD1 | MD1 | 46 | EOEN/ESSK | PPE | N.C |
| 7 | CD9 | N.C | MD9 | 47 | EWEN/ESDI | PERRN | N.C |
| 8 | CD2 | PD2 | MD2 | 48 | CD3 | PD3 | MD3 |
| 9 | CD10 | N.C | MD10 | 49 | CD4 | PD4 | MD4 |
| 10 | SOCN | | | 50 | CD11 | N.C | MD11 |
| 11 | XRT | | | 51 | CD5 | PD5 | MD5 |
| 12 | GND | | | 52 | GND | | |
| 13 | XCT | | | 53 | CD12 | N.C | MD12 |
| 14 | MODE0 /ESDO | MODE0 | MODE0 | 54 | CD6 | PD6 | MD6 |
| 15 | XRS | | | 55 | CD13 | N.C | MD13 |
| 16 | MODE1 | | | 56 | CD7 | PD7 | MD7 |
| 17 | LEDN | | | 57 | CD14 | N.C | MD14 |
| 18 | SWPDN | | | 58 | CCE1N | PSLCTIN | MCSN |
| 19 | SCLE | | | 59 | CD15 | N.C | MD15 |
| 20 | SCEN | | | 60 | CA10 | N.C | N.C |
| 21 | SALE | | | 61 | CCE2N | N.C | MBHEN |
| 22 | SREN | | | 62 | COEN | N.C | MOEN |
| 23 | GND | | | 63 | GND | | |
| 24 | SWEN | | | 64 | CIORDN | PALFN | N.C |
| 25 | SBUSYN | | | 65 | CA9 | N.C | N.C |
| 26 | SWPN | | | 66 | CIOWRN | PSTRBN | N.C |
| 27 | SD0 | | | 67 | CA8 | N.C | N.C |
| 28 | SLVD | | | 68 | CWEN | N.C | MWEN |
| 29 | SD1 | | | 69 | CIREQN | N.C | MIREQN |
| 30 | SD7 | | | 70 | CA7 | N.C | N.C |
| 31 | VDD | | | 71 | CA6 | N.C | N.C |
| 32 | SD2 | | | 72 | CA5 | N.C | N.C |
| 33 | VDD | | | 73 | VDD | | |
| 34 | SD6 | | | 74 | CRESET | N.C | MRESETN |
| 35 | SD3 | | | 75 | CA4 | N.C | N.C |
| 36 | GND | | | 76 | CWAITN | PBUSY | MWAITN |
| 37 | SD5 | | | 77 | CA3 | N.C | N.C |
| 38 | SD4 | | | 78 | CINPACKN | PACKN | N.C |
| 39 | SCDN | | | 79 | CA2 | N.C | MA2 |
| 40 | VENN | | | 80 | CREGN | PINIT | VDD |

NOTE: Nothing can be connected to NC pin.

4. Pin description

PC Card interface pin

| Pin Name | I/O | FUNCTION |
|----------|-----|--------------------------------------|
| CA0-CA10 | ID | Address Bus (11bit) |
| CD0-CD7 | BD | Data Bus-Low (8bit) |
| CCE1N | IU | Data Bus-Low Enable |
| CD8-CD15 | BD | Data Bus-High (8bit) |
| CCE2N | IU | Data Bus-High Enable |
| COEN | IU | Read Strobe for PC Card Memory Area |
| CWEN | IU | Write Strobe for PC Card Memory Area |
| CIORDN | IU | Read Strobe for PC Card I/O Area |
| CLOWRN | IU | Write Strobe for PC Card I/O Area |
| CIREQN | O | Interrupt Request |
| CRESET | IU | PC Card Reset |
| CWAITN | O | Wait Request From PC Card |
| CINPACKN | O | Input Acknowledge |
| CREGN | IU | PC Card Register Select |

SmartMedia interface pin

| Pin Name | I/O | FUNCTION |
|----------|-----|---|
| SD0-SD7 | BD | Media Data Bus (8bit) |
| SCLE | O3 | Media Command Latch Enable |
| SALE | O3 | Media Address Latch Enable |
| SWEN | O3 | Media Write Enable |
| SWPN | O3 | Media Write Protect |
| SCDN | IU | Card Detect (Pulled-up with 10K ohms) |
| SLVD | ID | Detect Operation Vcc Voltage (It usual needs to be Pulled-down with 10K ohms. In the case of automatic SmartMedia Vcc change, It does not need.) |
| SBUSYN | IU | Media Busy (Pulled-up with 2.4K ohms) |
| SREN | O3 | Media Read Enable |
| SCEN | O3 | Media Card Enable |
| SWPDN | IU | WP Label Detect (Pulled-up with 10K ohms) |
| VENN | O | SMARTMEDIA Vcc Control (It is "ON" when 'L') |

EEPROM interface pin (PC Card Mode)

| Pin Name | I/O | FUNCTION |
|-----------------|-------|--|
| ECSN/ESCS/EMODE | O/O/I | If this pin is 'H' during reset, the mode will be Parallel EEPROM mode and this pin will be EEPROM Chip Select. If this pin is 'L' during reset, the mode will be Serial EEPROM mode and this pin will be Serial EEPROM Chip Select. For more information on connection, refer to the description about EEPRPOM. |
| EOEN/ESSK | O/O | EEPROM Read Strobe or Serial EEPROM Clock For more information on connection, refer to the description about EEPRPOM. |
| EWEN/ESDI | O/O | EEPROM Write Strobe or Input Data to Serial EEPROM For more information on connection, refer to the description about EEPRPOM. |
| ESDO | I | Output Data from Serial EEPROM (Pulled-up with 2.4K ohms) For more information on connection, refer to the description about EEPRPOM. |

Parallel port interface pin

| Pin Name | I/O | FUNCTION |
|----------|-----|-----------------|
| PD0-PD7 | BD | Data Bus (8bit) |
| PACKN | O3 | Acknowledge |
| PBUSY | O3 | Busy |
| PPE | O3 | Paper Empty |
| PSLCT | O3 | Select |
| PERRN | O3 | Error |
| PSTRBN | I | Strobe |
| PALFN | I | Autofeed |
| PINIT | I | Initialize |
| PSLCTIN | I | Select In |

Micro controller bus interface pin (MPU bus mode)

| Pin Name | I/O | FUNCTION |
|----------|-----|----------------------|
| MD0-MD7 | BD | Data Bus Low (8bit) |
| MD8-MD15 | BD | Data Bus High (8bit) |
| MA0-MA2 | I | Address Bus(3bit) |
| MWAITN | O | Wait |
| MCSN | I | Chip Select |
| MBHEN | I | Bus High Enable |
| MIORN | I | Read |
| MIOWN | I | Write |
| RESETN | I | Reset |

Others

| Pin Name | I/O | FUNCTION |
|------------|-----|--|
| LEDN | O3 | Access Lamp Control It is 'L' for at least 50ms during Media access. |
| XIN | I | Connect to the pin of the 20MHz crystal oscillator. When the oscillator is not used, connect to VCC. For more information on connection, refer to the description about the oscillating circuit. |
| XOUT | B | Connect to the pin of the 20MHz crystal oscillator. This is also used for clock input from the oscillator. When CR oscillating is used, connect to GND. For more information on connection, refer to the description about the oscillating circuit. |
| XRS | I | When CR oscillating is used, connect to 10K ohms. When CR oscillating is not used, connect to VDD. For more information on connection, refer to the description about the oscillating circuit. |
| XRT | O | When CR oscillating is used, connect to 150 ohms. When CR oscillating is not used, open this. For more information on connection, refer to the description about the oscillating circuit. |
| XCT | O | When CR oscillating is used, connect to 15pF. When CR oscillating is not used, open this. For more information on connection, refer to the description about the oscillating circuit. |
| MODE0/ESDO | IU | Operation Mode Select |
| MODE1 | IU | MODE1:L MODE0:L 0 Parallel port mode MODE1:L MODE0:H 1 MPU bus mode MODE1:H MODE0:L 2 Setting forbidden MODE1:H MODE0:H 3 PC Card mode When the serial EEPROM is used at PC Card mode, pull up MODE0 at 10K ohms. |
| SOC | IU | SmartMedia Output Pin Function L:Open Collector H:CMOS 5V Drive For more information, refer to the description about SmartMedia and interface. |

Description about I/O I:Input O:Output U:500k ohm-pull-up D:500k ohm-pull-down 3:Tri-state

5. Operating mode

1. Setting of operating mode

Operating mode of the controller is set by statuses of MODE1 and MODE2 pin at reset.

| MODE1 | MODE0 | Operating mode |
|-------|-------|--------------------|
| L | L | Parallel port mode |
| L | H | MPU bus mode |
| H | L | Forbidden |
| H | H | PC Card mode |

NOTE:When the serial EEPROM is used at PC Card mode, pull-up MODE0 pin at 10k ohms.

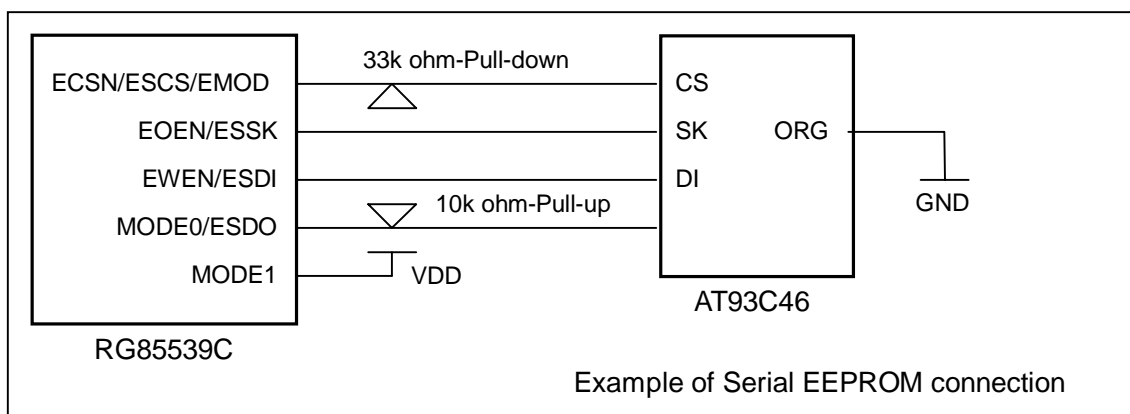
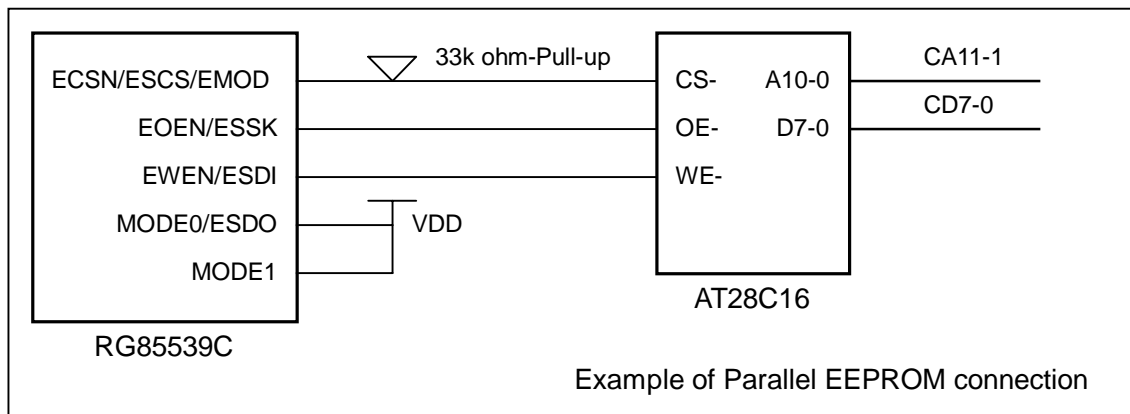
2. Setting of EEPROM mode

When PC Card mode, EEPROM is used as the memory where CIS is stored.

When the status of EMODE is 'H', EEPROM is Parallel EEPROM AT28C16(2k x 8bit,5V) mode.

When the status of EMODE is 'L', EEPROM is Serial EEPROM AT28C16(2k x 8bit,5V) mode.

The examples of connection are shown below:

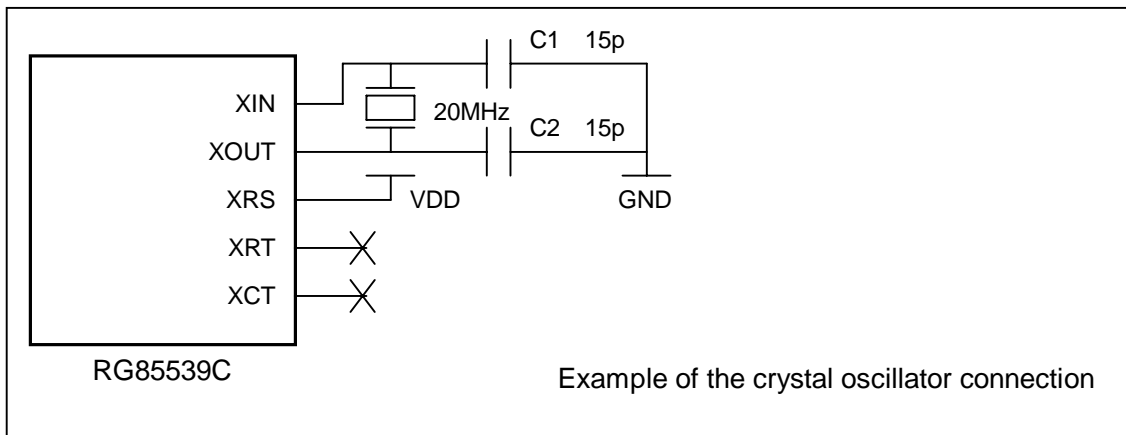


NOTE:The serial EEPROM is compatible with only 8-bit mode. Connect ORG pin to GND. AT93C46A for only 16-bit mode can not be used. Clock rate of ESSK pin is fixed as 2MHz.

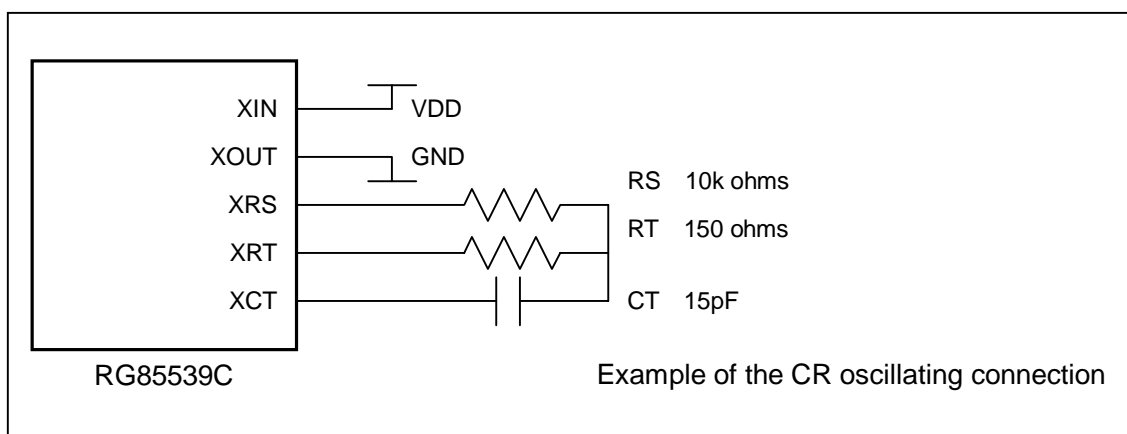
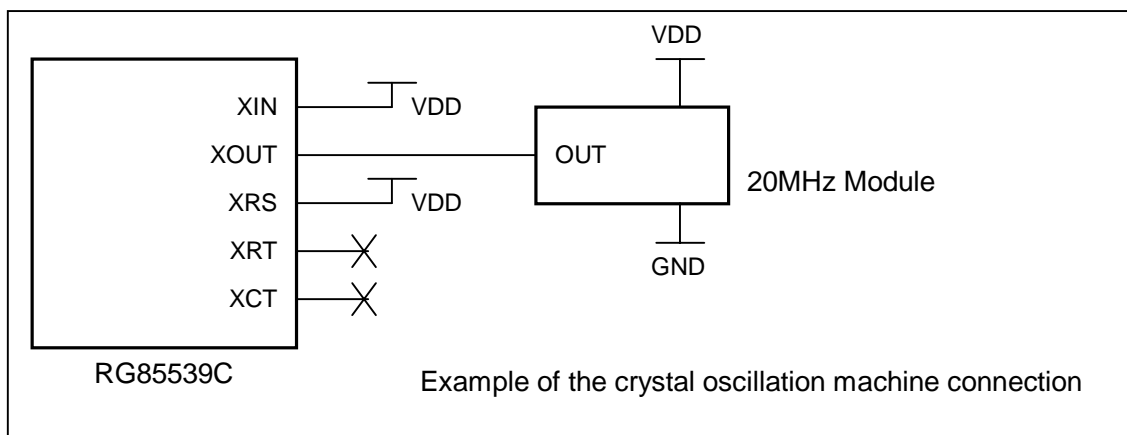
3. Selecting of oscillation circuit

Input 20MHz as clock to operate this controller. The oscillation circuit is selected from among the crystal oscillator, the crystal oscillation machine, and the CR oscillation.

The examples of connection are shown below:



Note : Values of C1,C2 are reference value. They may depend on the crystal oscillator or stray capacity of substrate. Layout the crystal units, C1 and C2 near the pins.



Note : Values of RT and CT are standard values at 20MHz. The frequency may depend on the stray capacity of substrate. When the frequency is adjusted, monitor it by XRT pin and make RT value changeable to from 20MHz -10% to 20MHz +10%. Layout RS, RT and CT near each pin. The XRS input signal must not be intersected with the XRT output signal because they are negative feedback. It may oscillate abnormally.

6. Register

1. Register map

At PC Card mode, these registers are located at any address in the Common Memory Space or the I/O Space by 8bytes boundary. At Micro Controller Bus mode, these are located in the I/O Space by 8bytes.

| Address | Register | R/W |
|---------|----------------|-----|
| +0 | DATA(Low) | R/W |
| +1 | DATA(High) | R/W |
| +2 | Status/Control | R/W |
| +3 | Signature | R/W |
| +4 | DATA(Low) | R/W |
| +5 | DATA(High) | R/W |
| +6 | DATA(Low) | R/W |
| +7 | DATA(High) | R/W |

At Parallel Port mode, these registers are located.

| Address | Register | R/W |
|---------|----------------|-----|
| L | DATA(Low) | R/W |
| H | Status/Control | R/W |

2. Data Register (R/W)

Address Offset +0, +1, +4, +5, +6, +7

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |

These registers are data port to SmartMedia. Write data to these registers are passed to SmartMedia and read data are passed from SmartMedia.

At PC Card mode and Micro Controller Bus mode, Byte access is available to +0, +4 and +6h. Word access is available to +0, +4 and +6h. Double Word access is available to +4h. Byte access to +1, +5, +7h is invalid.

At Parallel mode, Byte access (R/W) and Nibble access (R) are available. Please refer to the description about access at Parallel port mode.

3. Mode register (Write)

Address Offset +2h

| | | | | | | | |
|-----|--------|--------|----|------|------|-----|-----|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| -WP | (ECC1) | (ECC0) | CE | PWR1 | PWR0 | ALE | CLE |

This register is used to select SmartMedia data transfer mode.

-WP : Write Protect

'1' Disables the Write Protect (SWPN pin = H).

'0' Enables the Write Protect (SWPN pin = L).

ECC1,0 : Enable Hardware ECC (optional)

CE : SmartMedia Card Enable Control

'1' Card Enable (SCEN pin = L).

'0' Card Disable (SCEN pin = H).

PWR1,0 : SmartMedia Vcc Control

This controls the power supply to SmartMedia. When no SmartMedia is inserted (SCDN pin = H), Writing is invalid and Vcc is OFF (VENN pin = H).

| PWR1,0 | Power Supply to SmartMedia |
|--------|---------------------------------|
| 0,0 | VCC is kept in previous status. |
| 0,1 | Reserved |
| 1,0 | VCC OFF (VENN pin = H) |
| 1,1 | VCC ON (VENN pin = L) |

ALE : Address Latch Enable

'1' The data in data register is passed to SmartMedia as an Address (SALEN pin = L).

'0' The data in data register is passed to SmartMedia as Data (SALEN pin = H).

CLE : Command Latch Enable

'1' The data in data register is passed to SmartMedia as a Command (SCLEN pin = L).

'0' The data in data register is passed to SmartMedia as Data (SCLEN pin = H).

4. Status Register (Read)

Address Offset +2h

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|------|-------|----|-----|-------|------|-------|-----|
| BUSY | MODEL | - | PWR | STCHG | CENB | HWECC | WPD |

This register indicates a current status of SmartMedia.

BUSY : This bit indicates a current status of SmartMedia.

'1' SmartMedia is in BUSY status. (SBUSYN pin = L)

'0' SmartMedia is in READY status. (SBUSYN pin = H)

MODEL : This bit indicates a Power Requirement of SmartMedia.

'1' 5V Vcc is required.

'0' 3.3V Vcc is required.

PWR : This bit indicates a VCC status of SmartMedia.

'1' Vcc is provided.

'0' Vcc is removed.

STCHG : This bit indicates a event caused by SmartMedia media insertion or removal.

'1' The media insertion event or media removal event is occurred.

This bit is reset by writing operation to Mode Control Register.

CENB : This bit indicates a existence of SmartMedia card in the socket.

'1' SmartMedia media exists in the socket.

'0' SmartMedia media doesn't exist in the socket.

HWECC : This bit indicates the implementation of Hardware ECC.

'1' Hardware ECC is implemented.

'0' Hardware ECC is not implementd.

This is default value for our current chip.

WPD : This bit indicates existence of WP label on SmartMedia.

'1' WP label is stuck on the media.

'0' No WP label.

5. Signature Register (Read/Write)

Address Offset +2h

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----------|----|----|----|-----|----|--------|-------|
| 1 | 0 | 0 | 1 | 1 | 0 | RdyREQ | INTEN |
| Signature | | | | REV | | | |

This register controls the signature code and interrupt request of RG85539.

This register is valid when PC Card mode and MPU bus mode, invalid when Parallel port mode.

Signature : This bit indicates the signature code of RG85539.

'1001' is read. Writing to these bits is invalid.

REV : This bit indicates a revision of RG85539C.

'10' is read. Writing to these bits is invalid.

RdyREQ : This bit indicates that status of the SmartMedia is Ready.

'1' Status of the media turned from Busy to Ready.

This bit is reset by writing operation to Mode Register.

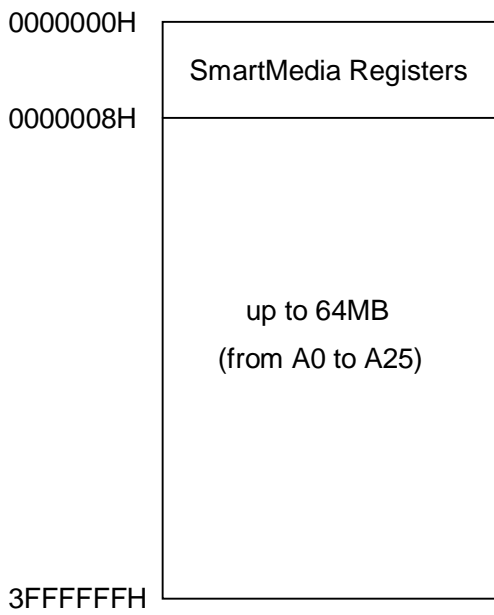
INTEN : This bit indicates that interrupt request is valid.

'1' Interrupt request to the host is permitted when RdyREQ or STCHG is '1'.

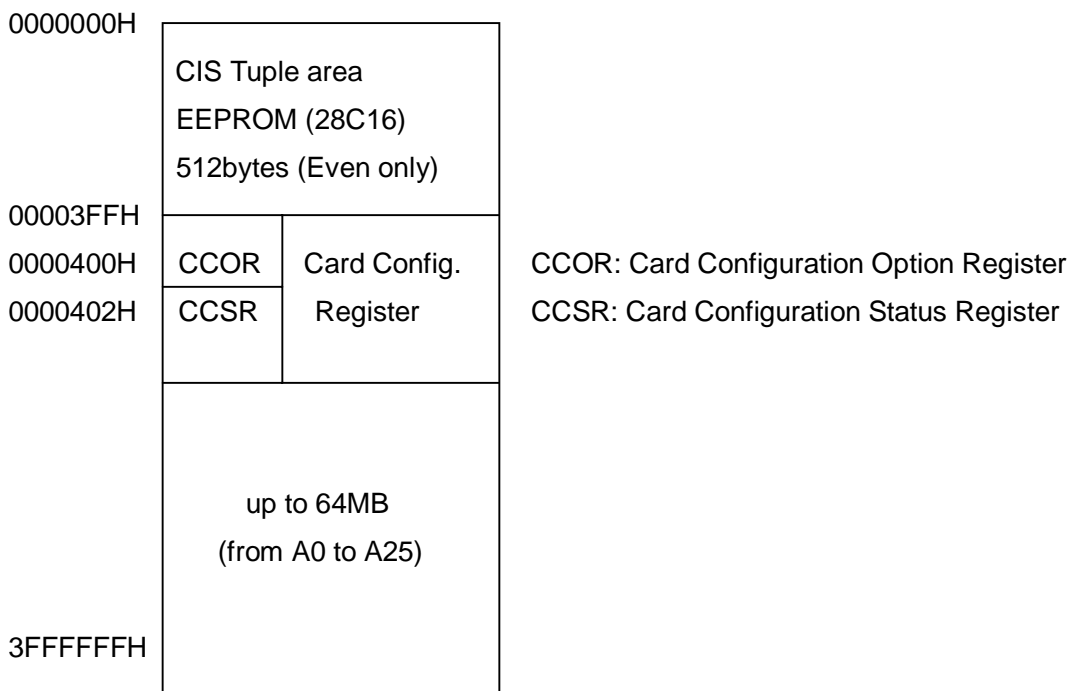
'0' At reset, this bit will turn to '0'.

7. PC Card mode

1. Common memory space (CREGN=H,COEN/CWEN=L)



2. Attribute memory space (CREGN=L,COEN/CWEN=L)



3. Card Configuration Register (CCR)

Card Configuration Register (CCR) is located at address from 400h to 402h in the Attribute Memory Space. CCR includes Option Register (CCOR) and Status Register (CCSR).

3-1. CCOR : Card Configuration Option Register

Located at address 400h in Attribute Memory Space

| | | | | | | | |
|--------|--------|-----|-----|-----|-----|-----|-----|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| SRESET | LvIIRQ | CI5 | CI4 | CI3 | CI2 | CI1 | CI0 |

SRESET 1 : Force Card Reset 0 : Release Card Reset

This bit is reset '0' after Power-On.

Write '1' to this bit forces the chip to reset state and should write '0' after the chip reset to start it.

LvIIRQ 1 : Level Interrupt mode 0 : Edge Interrupt mode

This bit is set to 1 after Power-On or Chip Reset.

This chip doesn't support the Edge Interrupt mode.

Therefore the value '0' is invalid

CI5-0 Configuration Index bit 5-0

| CI | I/O Space and I/O Function |
|--------|--|
| 543210 | |
| 000000 | Disable I/O function. (Default value after Reset) |
| 000001 | Independent I/O mode enable. +00h - +07h (A0 - A2 are decoded) |
| 001000 | I/O function is not available. |

3-2. CCSR : Card Configuration Status Register

Located at address 402h in Attribute Memory Space

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------|--------|-------|-------|-------|--------|------|-------|
| Chged | SigChg | IoIs8 | Rsvd0 | Audio | PwrDwn | Intr | Rsvd0 |

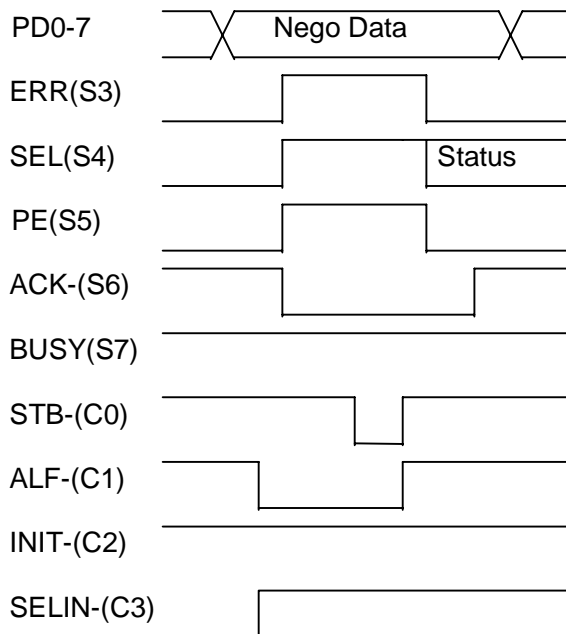
- Chged** This bit indicates the bit status change in Pin Replacement Register (PRR). This bit is not implemented to our chip. So, this bit is read-only and always returns '0'.
- SigChg** Write '1' to this bit enables -STSCHG(BVD1) signal. This bit is not implemented to our chip. So, this bit always returns '0'. Writing '1' to this bit is ignored.
- IOIs8** Set host (System) side bus wide.
1 : 16bit mode D15 to D0
0 : 8bit mode D7 to D0
Our chip always runs on 8bit Data bus (D7 to D0). So, this bit is read-only and always returns '0'. Writing '1' to this bit is ignored.
- Rsvd0** Reserved. This bit is read-only and always returns '0'.
- Audio** Enable and disable SPKR-(BVD2) output. This bit is not implemented to our chip. Therefore this bit is read-only and always returns '0'. Writing '1' to this bit is ignored.
- PwrDwn** Set Power Down mode. This mode is not implemented to our chip. Therefore this bit is read-only and always returns '0'. Writing '1' to this bit is ignored.
- Intr** Interrupt status bit. This bit is read-only and always returns '0'.
0 : Chip doesn't have an Interrupt request.
1 : Chip has an Interrupt request. This bit is holding until the interrupt request is serviced and removed.

8. Parallel port mode

The followings indicate flows in case of access by parallel mode.

1. Negotiation

The way to access of parallel port is specified by negotiation.



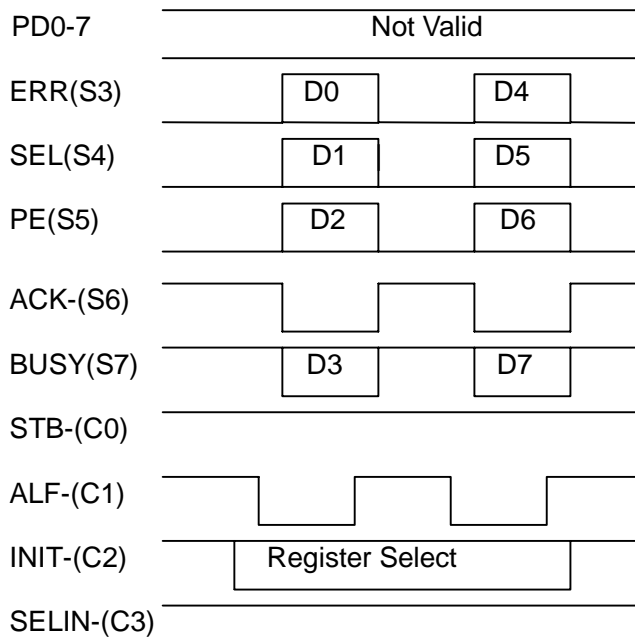
1. A host outputs negotiation data to PD0-7, sets SELIN- to 'H' and ALF- to 'L', and waits responses.
2. A host waits until ERR, SEL and PE turn to 'H' and ACK- to 'L'. If they are not these statuses, this device is not connected.
3. If there are responses, a host outputs STB- 'L' and sets ALF- and STB- to 'H' for 500nsecs
4. If device makes sure they turn to the above-mentioned status, it sets ERR and PE 'L', and returns the support status for the Negotiation Data to SEL. If it supports, device returns 'H'. If it doesn't support or operates by Nibble mode, it returns 'L'.

| Negotiation Data | Operation Mode | SEL |
|------------------|-------------------------------|-----|
| 00 | Nibble Mode / Byte Write Mode | L |
| 01 | Byte Read / Byte Write Mode | H |

5. After 500nsecs since support status, ACK- turns to 'H' and negotiation is finished.
6. After this, the data access by the negotiated mode while SELIN- is 'H' is available.
If SELIN- is turned to 'L', it needs to negotiate again.

2. Nibble read

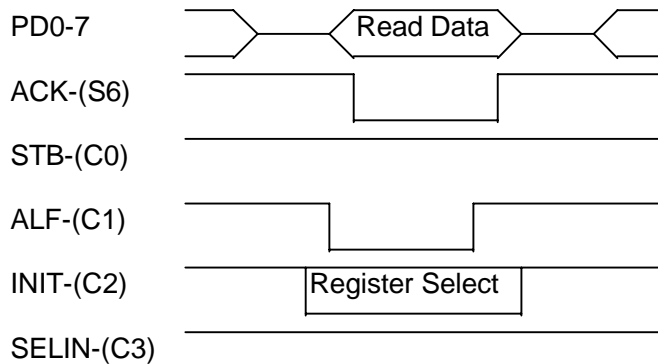
The following indicates the way to read by Nibble mode. This is available after Nibble mode negotiation succeeds.



1. SELIN- needs to keep 'H'. STB- needs to keep 'H' at access. PD0-7 is not implemented to our chip.
2. The accessed register is specified by INIT-. 'L' indicates Data Register. 'H' indicates Status Register.
3. If ALF- is set to 'L', D0, D1, D2 and D3 are output ERR, SEL, PE and BUSY, and ACK- turns to 'L'.
4. After a host makes sure ACK- turns to 'L', reads low nibble data.
5. If ALF- is turned to 'H', ERR, SEL, PE, BUSY and ACK- turn to the former status and reading nibble data is finished.
6. If nibble data is read continuously, D4, D5, D6 and D7 is output to ERR, SEL, PE and BUSY. INIT- must not be changed.
7. Data is output in order of the low-data and the high-data every reading nibble data.

3. Byte read

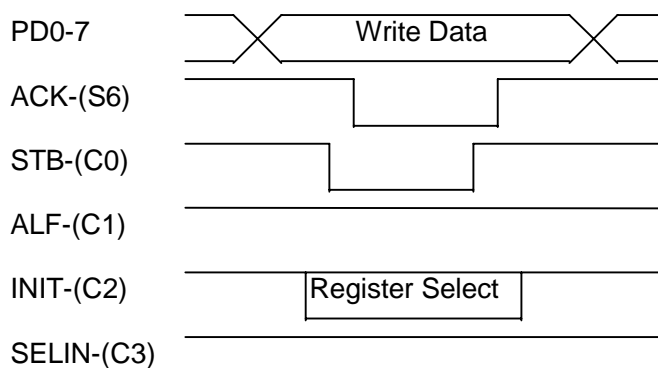
The following indicates the way to read by Byte mode. This is available after Byte mode negotiation succeeds.



1. SELIN- needs to keep 'H'. STB- needs to keep 'H' at access. ERR,SEL,PE and BUSY are not implemented to our chip.
2. Set the direction of PD0-7 Read mode.
3. The accessed register is specified by INIT-. 'L' indicates Data Register. 'H' indicates Status Register.
4. If ALF- is set 'L', byte data is output to PD0-7 and ACK- turns to 'L'.
5. A host makes sure ACK- turns L' and reads byte data.
6. If ALF- is turned to 'H', ACK- turns to 'H'. If the direction of PD0-7 is turned to Output, reading is finished.

4. Byte write

The following indicates the way to write by Byte mode. This is available after either Nibble mode or Byte mode negotiation succeeds.



1. SELIN- needs to keep 'H' since negotiation. ALF- needs to keep 'H' at access. ERR,SEL,PE and BUSY are not implemented to our chip.
2. Data written to PD0-7 is output.
3. The accessed register is specified by INIT-. 'L' indicates Data Register. 'H' indicates Control Register.
4. If STB- is turned to 'L', ACK- turns to 'L'.
5. A host makes sure ACK- turns to 'L' and turns STB- to 'H', ACK- turns to 'H' and writing is finished.

9. Interface with SmartMedia

RG85539C supports 5V mode and 3.3V/5V mode interfaces.

1. 5V mode

The interface is turned to 5V mode by connecting SOCN pin with VDD. SmartMedia interface signal is driven with COMS level. When it is connected with SmartMedia directly, only 5V SmartMedia is available.

2. 3.3V/5V mode

The interface is turned to 3.3V/5V mode by connecting SOCN pin with GND. SmartMedia interface signal is driven with Open Drain. When it is pulled up to the changeable SmartMedia power supply, both 3.3V and 5V SmartMedia are available.

10. Electrical characteristics

1. Absolute Maximum Ratings

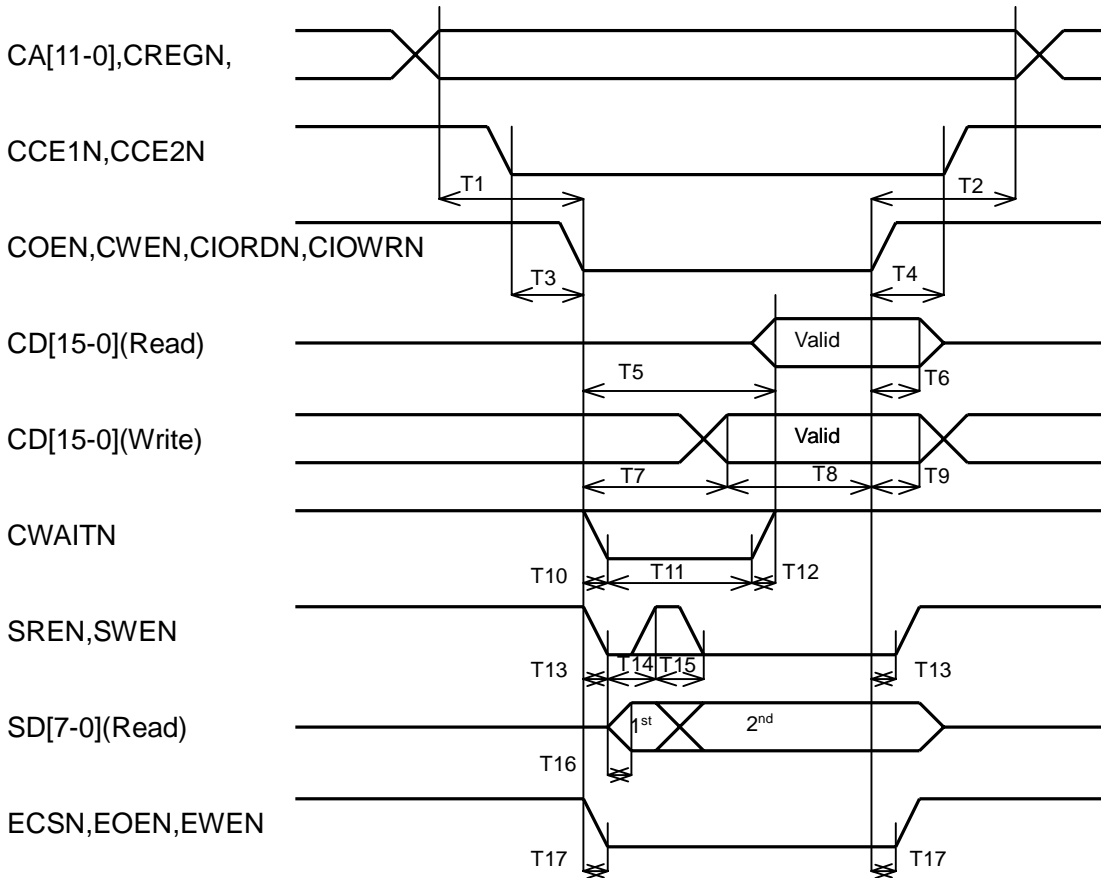
| RATING | SYMBOL | VALUE | UNIT |
|----------------------|--------|-------------------------|------|
| Power Supply | VDD | From GND-0.5 to 6.0 | V |
| Input Voltage | VIN | From GND-0.5 to VDD+0.5 | V |
| Output Voltage | VOUT | From GND-0.5 to VDD+0.5 | V |
| Output Current / Pin | IOUT | From -30 to +30 | mA |
| Storage Temperature | TST | From -55 to +125 | C |

2. Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--------------------|--------|------|------|------|------|
| Power Supply | VDD | 4.75 | 5.00 | 5.25 | V |
| Input Voltage | VIN | GND | - | VDD | V |
| Around Temperature | Ta | 0 | 25 | 70 | C |

9. AC Characteristics

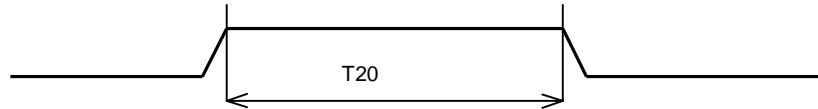
1. Common Memory / Attribute Memory / I/O Timing



| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------|--|-----|-----|------|
| T1 | Address Set-Up Time to COEN CWEN CIORDN CIOWRN Low | 10 | | ns |
| T2 | Address Hold Time from COEN CWEN CIORDN CIOWRN High | 15 | | ns |
| T3 | CE Set-Up Time to COEN CWEN CIORDN CIOWRN Low | 0 | | ns |
| T4 | CE Hold Time from COEN CWEN CIORDN CIOWRN High | 15 | | ns |
| T5 | Read Data Enable Time from COEN CIORDN | 5 | 65 | ns |
| T6 | Read Data Hold Time from COEN CIORDN | 5 | | ns |
| T7 | Write Data Set-Up Time from CWEN CIOWRN (At Writing to Register and Word Writing to SmartMedia) | 20 | | ns |
| T8 | Write Data Set-Up Time to CWEN CIOWRN (At Writing to CIS and Byte Writing to SmartMedia) | 100 | | ns |
| T9 | Write Data Hold Time from CWEN CIOWRN | 15 | | ns |
| T10 | CWAIT Low Delay Time (At Word Access to SmartMedia) | | 15 | ns |
| T11 | CWAIT Low Time (At Word Access to SmartMedia) | | 300 | ns |
| T12 | CWAIT High to Read Data Effective (At Word Read to SmartMedia) | | 0 | ns |
| T13 | SREN SWEN Delay Time | | 15 | ns |
| T14 | SREN SWEN First Byte Access Time (At Word Access to SmartMedia) | 100 | | ns |
| T15 | SREN SWEN First Byte and Second Byte Interval Time (At Word Access to SmartMedia) | 100 | | ns |
| T16 | Read Data Access Time from SREN Low (At Word Access to SmartMedia) | | 80 | ns |
| T17 | ECSN EOEN EWEN Delay Time | | 15 | ns |

2. Reset Timing

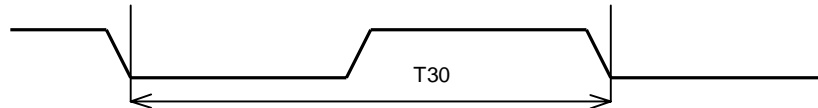
CRESET



| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------|-------------------|-----|-----|------|
| T20 | Reset High Period | 12 | | ns |

9.3 Clock Timing

CLKIN



| SYMBOL | PARAMETER | MIN | NOMAL | MAX | UNIT |
|--------|-----------------|-----|-------|-----|------|
| T30 | Clock Cycle | | 50 | | ns |
| fclk | Clock frequency | | 20 | | MHz |

10. Appendix

Size of Package

Size of Package

